

## **REMARKS**

Applicant thanks Examiner for the detailed review of the application and the suggestion for a direction of potential allowable subject matter.

### **Claim Objections**

Claims 1 and 35 have been amended to rectify the antecedent basis problems regarding introduction of an OS. Claim 1 has also been amended to recite, “non-privileged, user-level programming instruction,” at each use thereof. In claim 17, “to” has been added for clarity. In claim 51, the abbreviation of OS is defined. Claim 55 has been amended to “a plurality of user-level threads,” to provide proper antecedent basis.

### **Claim Rejections -35 USC § 102(b)**

10. Claims 1-2, 4-7, 9-12, 15-17, 20, 22-25, 27-28, 32, 35-43, 47, 50-51, 55-58, 62-65, 67-68, and 70-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Kissell (USPN 7,376,954).

As The Office Action suggested, the use of a shared register for communication has been included in some form within the applicant’s independent claims—1, 17, 35, 51, 55, and 67. The Office Action cites Kissell’s Thread Control Register of CP0. Note that Kissell’s thread control register is disclosed as only including an AlternateThread field to indicate which thread context is to be accessed by the MTTR instruction (See col. 12 lines 35-49). However, the thread control register is not shared—accessible to each—for communication, but rather is accessed as conventional, **privileged** resources (See col. 13 lines 34-40). For example, Kissel does not disclose a first shred communicating to a second shred through a shared register, such as one shred writing to the register and the other shred reading the register, as in applicant’s claims including such

elements.

Therefore, applicant respectfully submits that independent claims 1, 17, 35, 51, 55, and 67, as well as their dependent claims, are now in condition for allowance for at least the reasons stated above. If there are any additional charges, please charge Deposit Account No. 50-0221.

Respectfully submitted,  
Intel Corporation

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